Application No.: 10/661,486 Docket No.: 8734.231.00

Amendment filed on September 27, 2005 Reply to Office Action dated June 28, 2005

## **REMARKS**

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated June 28, 2005 has been received and its contents carefully reviewed.

Claims 1 and 4 are hereby amended. Claims 1–23 are pending. Claims 8-23 are withdrawn from consideration and claims 1-7 are examined. Reexamination and reconsideration of the examined claims are respectfully requested.

In the Office Action, claim 1 is rejected under 35 U.S.C. § 112, second paragraph. The Examiner states at page 2 of the Office Action that there is insufficient antecedent basis for the limitation "the etched semiconductor layer" in claim 1. Applicant herein amends claim 1 to overcome the rejection. Accordingly, Applicant respectfully requests withdrawal of this rejection.

Furthermore, in the Office Action, claims 1 and 4-7 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,573,163 to Voutsas et al. (hereinafter "Voutsas"). Claims 2 and 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Voutsas.

The rejection of claims 1 and 4-7 as being anticipated by Voutsas is respectfully traversed and reconsideration is requested.

Claim 1 is allowable over Voutsas in that the method of claim 1 recites a combination of elements including, for example, "partially etching the crystallized semiconductor layer to a second thickness less than the first thickness; and crystallizing the partially etched semiconductor layer in a second direction." Voutsas does not teach at least these features of the claimed invention. Specifically, the method of claim 1 of the present application is different from the method of Voutsas in that present claim 1 recites "crystallizing the partially etched semiconductor layer in a second direction." In contrast, Voutsas teaches crystallizing a first region of amorphous silicon such that the region has a first crystal orientation and then crystallizing a second different region of the amorphous silicon such that the second different region has a second crystal orientation. Column 3, lines 20-35. Voutsas teaches a crystallization

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method where a mask is repeatedly moved across an amorphous silicon region so as to form a first crystal orientation region. Then the crystallization method is repeated across a *different* region of the amorphous silicon using a second mask so as to form a second crystal orientation region. Column 6, lines 5-30; Figure 7. Therefore, Voutsas merely teaches crystallizing two different regions of amorphous silicon such that the different regions have different crystal orientations. Thus, Voutsas does not teach "partially etching the crystallized semiconductor layer to a second thickness less than the first thickness; and crystallizing the partially etched semiconductor layer in a second direction." Accordingly, because Voutsas fails to teach these features of claim 1, Applicant respectfully submits that claim 1 and claims 4-7, which depend therefrom, are allowable over Voutsas.

The rejection of claims 2 and 3 as being unpatentable over Voutsas is respectfully traversed and reconsideration is requested.

As discussed above, Voutsas does not teach or suggest "partially etching the crystallized semiconductor layer to a second thickness less than the first thickness; and crystallizing the partially etched semiconductor layer in a second direction," as recited in independent claim 1. Voutsas does not contain any further teachings or suggestions to cure the deficiencies as discussed above with regard to independent claim 1. For at least this reason, claims 2 and 3, which depend from claim 1, are allowable over Voutsas.

Applicant believes the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

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The undersigned hereby signs this filing under the authority provided by 37 C.F.R. §1.34 pending the filing of a Power of Attorney and Statement under 3.73(b) executed by Assignee.

Dated: September 27, 2005

Respectfully submitted,

Valerie P. Hayes

Registration No.: 53,005

McKENNA LONG & ALDRIDGE LLP

Docket No.: 8734.231.00

1900 K Street, N.W. Washington, DC 20006 (202) 496-7500

Attorney for Applicants